

Errata for FM25256 & FM25L256

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Errata Number 003 (all Date Codes)
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Product Marking FM25256 and FM25L256 (all package types)

Testing has identified a problem with FM25256 and FM25L256 devices that relates to slow write cycles. Write errors (typically single bit errors) may occur if (a) SCK operates below 200KHz or (b) SCK is suspended between the 5th and 8th clock of a write cycle or (c) /HOLD is asserted between the 5th and 8th clock of a write cycle. Reads are unaffected by these conditions because the read data is pre-fetched into a register at the beginning of the read operation, and the memory array is closed automatically by a self-timed circuit.

The following describes the internal operation of the 256Kbit SPI FRAM memories. These parts are designed to support serial data rates in excess of 20 MHz, however there is a limitation at very low speeds. The SPI operations are byte oriented and are initiated on the falling edge of /CS. The following diagram shows a write operation and includes the internal signal "Memory Access" to show when the memory array is accessed. For each data byte the array is accessed on the 5th clock and is closed on the 8th clock.

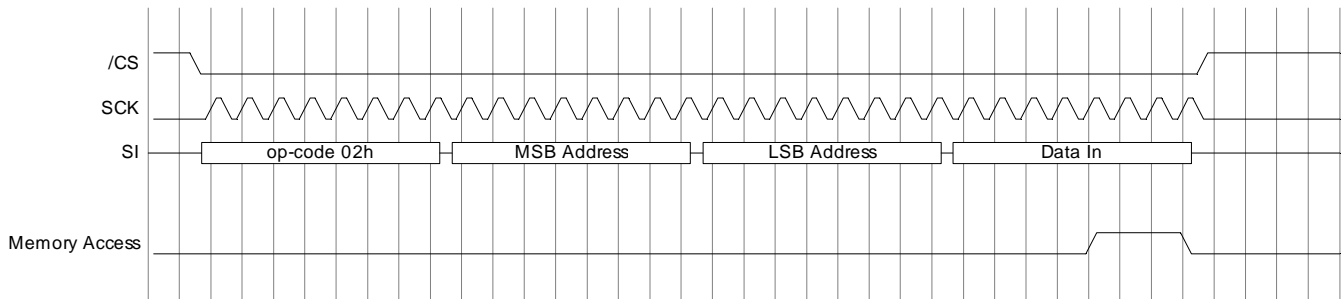


Figure 1. Write Operation Starts on 5th Clock and Completes on 8th Clock

For write operations the length of time the array is being accessed is a function of clock frequency, a temporarily stopped clock, and the time /HOLD is asserted. Testing has identified an errata condition for the FM25256 and FM25L256 devices. Current product versions have a timing constraint that the user must comply with – it is labeled "Internal Access Time" in the diagram below. The minimum time is 120ns (3 clocks at 25MHz) and the maximum time is 15 μ s. The maximum time of 15 μ s is exceeded if the clock frequency is lower than 200KHz, assuming a free-running clock and the /HOLD pin is not used within the memory access period.

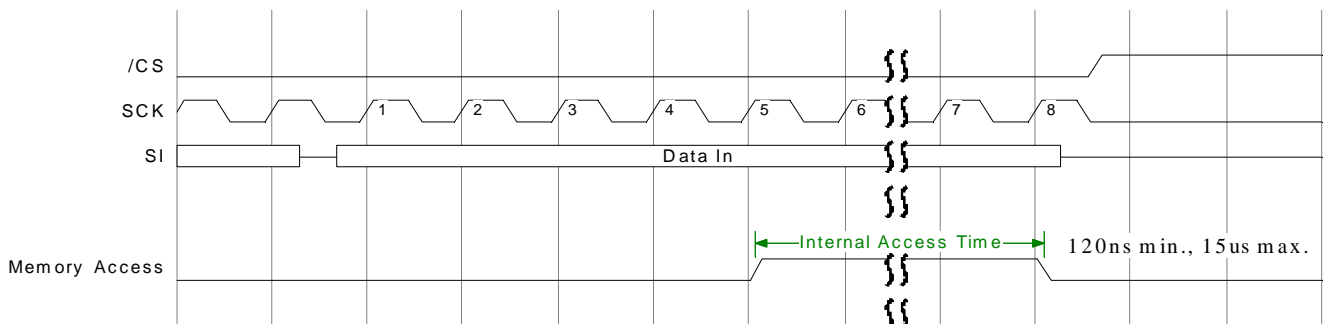


Figure 2. A Detailed Look at the Internal Memory Access and Timing Constraint

NOTE: The above issue will be resolved with the next die revision. Samples will be available in 3Q05.