

# Errata for FM25CL64



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**Errata Number** 001 (rev. AB)

**Date** Dec. 10, 2001

**Product Marking** FM25CL64

Recent testing has identified a few problems with the 64Kb SPI FRAM.

1)

Problem:	The maximum SCK operating frequency $f_{CK}$ does not meet the 20MHz spec but instead can be operated up to 10MHz.
Fix:	

2)

Problem:	Although the device operates at 10MHz, the clock high time $t_{CH}$ during status register write cycles must be relaxed to 60ns. (The clock low time $t_{CL}$ complies with the spec.)
Fix:	

3)

Problem:	Two input hold time parameters do not comply with the spec. The data input hold time $t_H$ must be relaxed to 5ns, and the chip select hold time $t_{CSH}$ must be relaxed to 15ns.
Fix:	

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NOTE: All of the above issues will be resolved with a rev. AD device. Samples will be available in late 1Q02.