

Errata for FM20L08

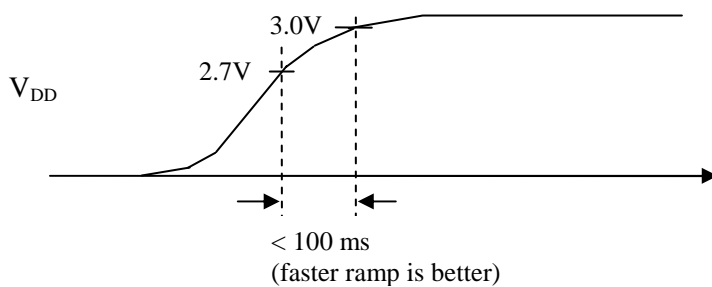
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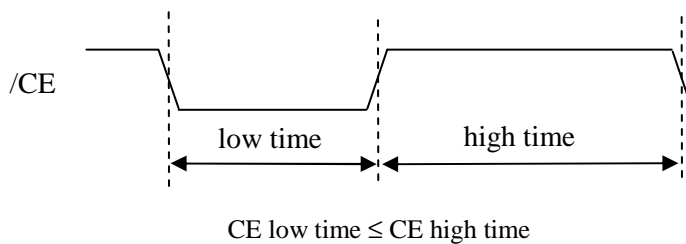
Errata Number	002 (Rev AD)
Date	Jan. 24, 2005
Product	1Mbit FRAM, 128Kx8
Product Marking	FM20L08-60 (all package types)

Initial testing has identified some problems with FM20L08 rev AD samples. The new die revision complies with the datasheet FM20L08ds_r0.8.pdf except for the following:

- 1) If the V_{DD} power-up ramp is too slow, the chip will lock out the user. V_{DD} must transition faster than 100 ms from 2.7V to 3.0V. See diagram below.



- 2) $/CE$ restrictions: $/CE$ low time $\leq 10 \mu s$ and $/CE$ low time \leq /CE high time.



NOTE: The above issues will be addressed with a future device revision.