

# Errata for FM20L08

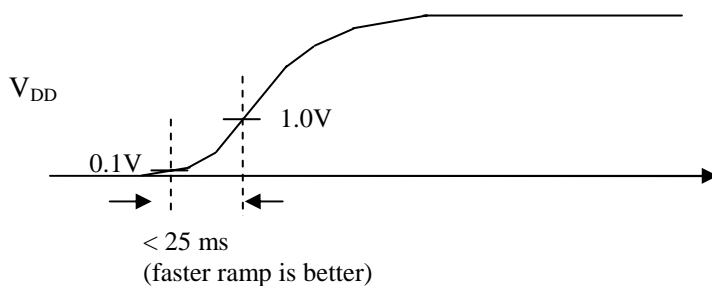
## RAMTRON

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<b>Errata Number</b>	003a (applies to Date Codes 0521 through 0605)
<b>Date</b>	Feb. 15, 2006
<b>Product</b>	1Mbit FRAM, 128Kx8
<b>Product Marking</b>	FM20L08-60-TGC (commercial temperature)

Initial testing has identified a problem with recent FM20L08 samples. These parts comply with the datasheet [FM20L08TC\\_r1.5.pdf](#) except for the following:

- 1) If the  $V_{DD}$  power-up ramp is too slow, the chip will not function properly.  $V_{DD}$  must transition faster than 25 ms from 0.1V to 1.0V. See diagram below.



- 2) The read cycle time  $t_{RC}$  and the write cycle time  $t_{WC}$  are 600 ns min. There are some workarounds that allow cycling the part as fast as the current specification (150ns for commercial grade). Please submit your requirements (access time and cycle time) to [framinfo@ramtron.com](mailto:framinfo@ramtron.com) and Ramtron's technical staff will provide alternative solutions.

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NOTE: The above issues have been addressed with a new die revision, which are now available as engineering samples. These are marked D/C 0606 and beyond.