Errata for FM20L08

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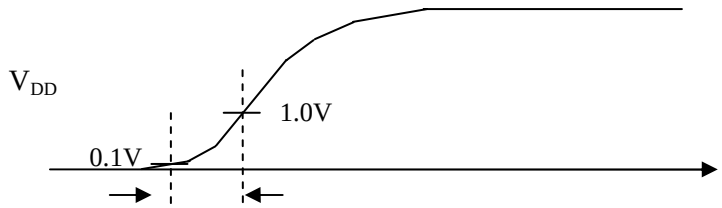
Errata Number	003c (applies to Date Codes up to 0605)
Date	Feb. 15, 2006
Product	1Mbit FRAM, 128Kx8
Product Marking	FM20L08-60-TG (extended temperature)

Testing has identified a problem with extended temperature FM20L08 samples. These parts comply with the datasheet FM20L08T_r1.4.pdf except for the following:

1) If the V_{DD} power-up ramp is too slow, the chip will not function properly. V_{DD} must transition faster than 15 ms from 0.1V to 1.0V. See diagram below.



< 15 ms (extended temp.)
Faster ramp is better.

2) If a particular block (32 rows each) in the memory array is accessed repeatedly more than 10,000 times, the device will exhibit bit errors within that same block. Bit errors are most likely to occur above 70°C. The problem can be eliminated by scanning the entire memory after 10,000 accesses. A "scan" routine may be written to perform a single read to each row. Since the FM20L08 memory array is organized as 16K rows of 8-bytes each, a routine that reads address 00h, 08h, 10h, 18h, 20h, … 1FFF0h, 1FFF8h will eliminate the problem. The entire memory scan is completed in 5.7 ms at a cycle time of 350 ns. There may be better scan methods for your particular system – please contact Ramtron at framinfo@ramtron.com to discuss this further.

NOTE: The above issues have been addressed with a new die revision, which are now available as engineering samples. These are marked D/C 0606 and beyond.