by **Mike Alwais**

FRAM TECHNOLOGY PUTS THE "INTELLIGENCE" IN SMART AIRBAG SYSTEMS

Safety systems for automobiles are expected to become more sophisticated over the next several years. A principal driver of this trend is expected regulation that will impact the attach rate and the sophistication of airbags and stability control systems. The electronic content of these systems will increase and with it, the demand on the semiconductor memory used in these systems. This article is a brief look at what to consider when choosing a memory solution for the newer classes of airbag.

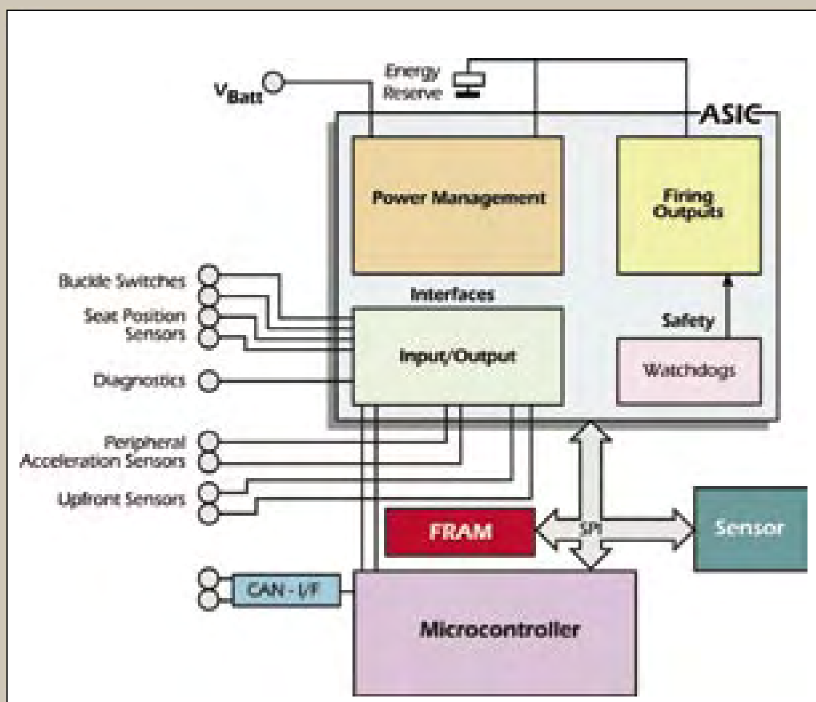

Figure 1. In an airbag system, SPI communication with FRAM allows the storage of sensor and system data.

Two major innovations are occurring in the airbag system. First, in newer airbag systems, "intelligence" is being added. Instead of deploying as in the past with maximum force as if all accidents and passengers were the same, deployment force is being determined by specific accident and occupant parameters. These may include the severity of the crash, the weight of the occupant and the seat position relative to the airbag. Those who have been hit by a standard airbag will consider variable force a positive. The smart airbag also knows that if the passenger seat is empty, the passenger airbag does not need to deploy. Given the increased number of airbags per vehicle and the cost of replacing them in even a minor accident, this innovation has the potential to provide the consumer with substantial cost savings in repairs and insurance.

A second innovation is that vehicles are increasingly being fitted with event data recorders (EDR's) that collect crash information similar to an airplane "black box." The EDR function is normally included in the airbag electronic control unit (ECU). This is a natural grouping because the EDR does not have the survivability requirements of an airplane "black box" and the airbag controller is the primary recipient of a variety of important sensor inputs. Vehicle makers are also quick to point out that there is no room for a stand-alone EDR.

The memory requirements of these two airbag memory applications are demanding but quite different. Both need a non-volatile memory because in all likelihood the power will be lost at some point during a serious accident. Reconstructing the event means that the data must be stored in a robust non-volatile memory that can be written in the system. Figure 1 shows the block diagram of a basic airbag system with FRAM memory storage.

In the case of a "smart airbag" the ECU designer wants to deploy the airbag with the appropriate force for a given accident. This requires not only information about the G forces but also about the occupant. A unique requirement for the memory in a smart airbag is to record the occupant history leading up to the event. This includes seat position and occupant weight. In order to keep a reliable record of the occupant profile prior to any event, it is necessary to continuously store that information. The parametric data that is sent to the airbag ECU is generated by accelerometers and sensors from the vehicle's interior. This continuous storage calls for a memory technology that can be written far more often than conventional flash memory.

In the case of an EDR, the challenge is related to the amount of data that is desired and the time available to store it. New regulations are expected to greatly expand the data set that is to be captured. When a serious accident occurs the power is most likely to be lost. In this case, the EDR system is in a race to store the data before energy is lost from the system. In an accident, power will often fail suddenly and the conventional non-volatile storage solutions take too long to program new information.

FRAM offers a technological solution to meet both challenges. Like other alternatives, it provides reliable non-volatile storage. The main distinctions are its high write endurance--it can be written a large number of times--and its write speed.

Popular choices for airbag applications are 5 V operation serial peripheral interface (SPI) FRAM memories. These devices provide write endurance of more than one trillion writes (one with twelve zeros). This is more than adequate to allow the smart airbag to write continuously, providing a seamless record of occupant data. These parts also write at bus interface speed.

Running between 5 MHz and 20 MHz with NoDelay writes enables the host processor to stream data as quickly as possible with little risk of losing information. Non-volatility, unparalleled write endurance coupled with fast data-collection capability make FRAM an ideal memory technology for the next generation of advanced airbag systems.

Previously, the predominant non-volatile memory technologies used in automotive applications were floating gate devices such as EEPROM or flash. Floating gate devices have polysilicon gates isolated from the channel by a thin SiO2 layer. To program a device, a high voltage is generated on the control gate to accelerate the electrons (N-channel device) toward the source. As a result, the electrons gain sufficient kinetic energy to penetrate the insulating layer and are trapped in the polysilicon material (Figure 2).

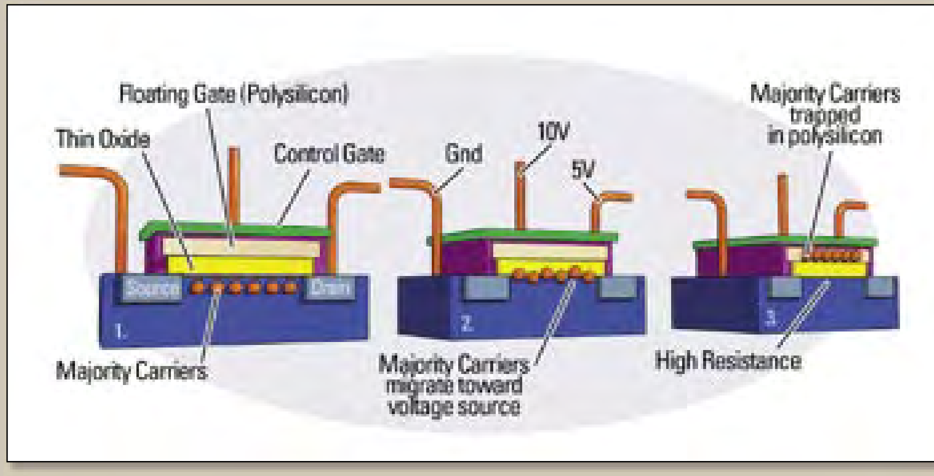

Figure 2. In the FRAM structure, a programmed device is "off" and has a higher resistance. A device that is not programmed or erased is "on" and has a lower resistance.

A depletion region is formed in the channel such that, at a particular gate voltage, a device that is programmed is "off" (higher resistance) and a device that is not programmed or erased is "on" (lower resistance).

As the complexity of automotive design requirements increases, the restrictive nature of floating gate memory technology becomes more apparent. For example, the programming process takes several milliseconds, which is an inordinately long time for safety-critical applications. In the kind of fast power outage that occurs in a crash, little information could be stored successfully in a floating gate device.

The programming process is also destructive to the insulating layer and such devices consequently have limited write endurance of typically 100,000 to 1,000,000 writes. In an occupant sensor, for example, data is updated too often for this upper limit. Given a typical requirement to write data once per second, a floating gate device would wear out in less then 12 days of operation. Buffering the data in RAM and writing to a floating gate non-volatile memory on power down introduces the speed problem that occurs in the EDR, not really a solution.

In smart airbag systems, it is not only necessary to store data in the event of a crash, but also desirable to store pre-crash data prior to an event. Using a rolling log to store pre-crash data is ideal, but this solution proves problematic for floating gate memory devices because of their limited endurance. Since airbag modules have large capacitors that store sufficient energy to fire the airbag, there may be sufficient residual energy to write the data from a buffer after the squib has fired. The amount of data that can be written is limited by the energy available, that is to say the residual energy in the capacitor and the speed with which the memory can be written. A typical 2 Kbyte floating gate memory device can write approximately 4 bytes/5 ms. To write an entire floating gate memory device, therefore, can take more than a second.

Using FRAM offers a solution. Its high endurance and speed solve both problems effectively. Ramtron's FRAM technology integrates ferroelectric materials with standard semiconductor chip design and fabrication technology to provide non-volatile memory and analog/mixed-signal products. These products combine the high-speed read/write performance, nearly unlimited write endurance and low power consumption of static RAM (SRAM) with the secure storage of data in the event of power loss that is unavailable with standard RAM technologies.

A FRAM cell is fabricated with an industry-standard complementary metal oxide semiconductor (CMOS) process, with a ferroelectric crystal between two electrode plates

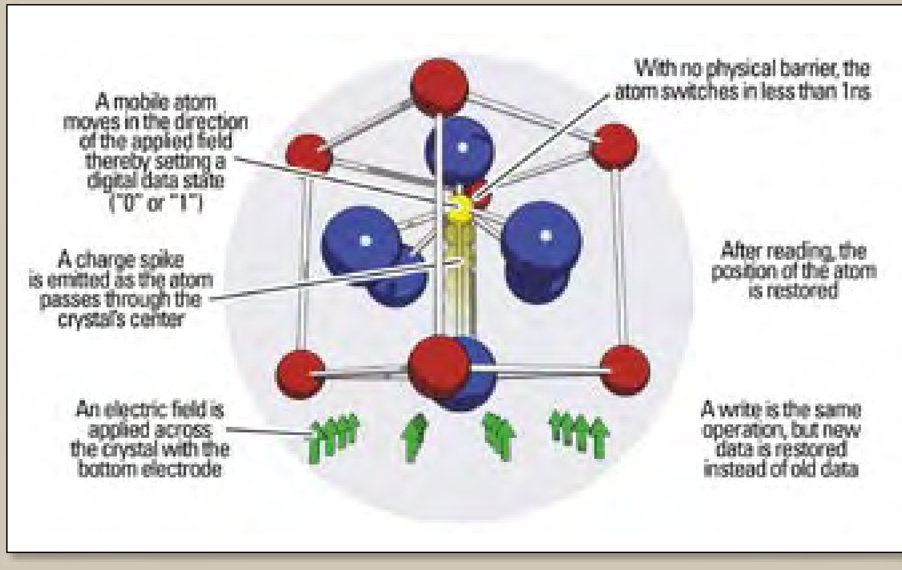

Figure 3. The ferroelectric crystal structure in an applied electric field.

to form a capacitor, similar in construction to a DRAM capacitor. Rather than storing data as a charge on the capacitor as volatile memories do, FRAM stores data within the ferroelectric crystal.

When an electric field is applied to a ferroelectric crystal the central atom moves in the direction of the field. As the atom moves within the crystal, it passes through an energy barrier, causing a charge spike. Internal circuits sense the charge spike and set the memory. If the electric field is removed from the crystal, the central atom stays in position, preserving the state of the memory. (Figure 3).

The ferroelectric thin film is placed over CMOS base layers and sandwiched between two electrodes. Metal interconnect and passivation complete the process (Figure 4).

Therefore, the FRAM memory needs no periodic refresh and when power fails, it retains its data. It is fast, and to all intents and purposes, it doesn't wear out. These properties make it adequate to write data at intervals of sufficient granularity to ensure the proper state is saved. For example, a 16 Kbit (2 Kbyte) device can be written in 3.3 ms with significantly lower power overhead. Alternately, it could be updated 10,000 (one write per 100 microseconds) times per second for a 25,000-hour operating life.

The recent decision by Hyundai Autonet to use non-volatile ferroelectric random access memory (FRAM) devices in its next-generation smart airbag systems is further evidence of the growing acceptance of the benefits of FRAM technology amongst leading automotive systems suppliers for use in such safety-critical applications. In this respect, Hyundai Autonet joins eight other automotive manufacturers across the United States, Asia, Japan and Europe that have opted for FRAM technology to provide the "intelligence" for smart airbag systems and associated crash event data recorders. ■

ABOUT THE AUTHOR

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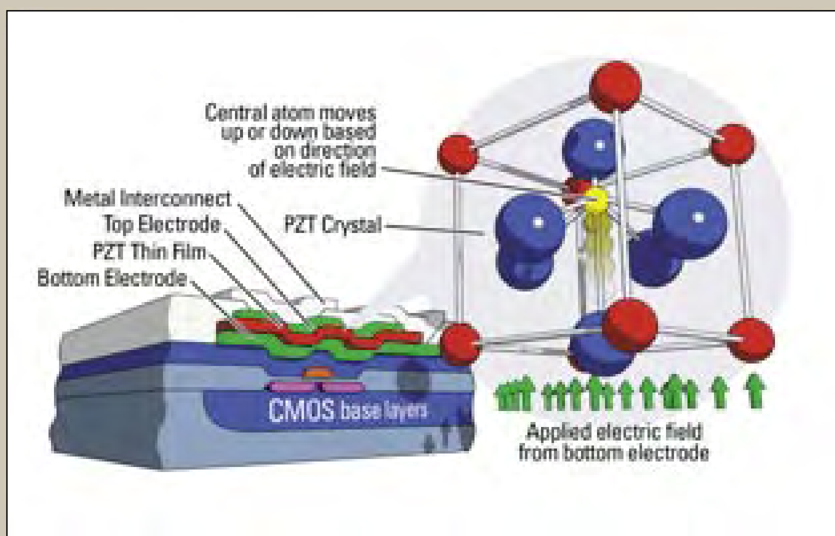

Figure 4. The ferroelectric material in a CMOS process.