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PRODUCT HOW-TO: Using Ramtron Non-volatile Memory For Tamper Detect In Meters

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Today's designers of utility meters and data collection systems face complex demands as the need for sophisticated utility distribution management grows.

Whether you are involved with the design of AMR (automatic meter reading), power quality meters, or energy monitoring systems for water, natural gas, or electricity utility systems, ferroelectric random access memory (F-RAM) offers the system a way to write data to non-volatile storage instantaneously. Floating gate technologies (EEPROM and Flash) use a write-back page buffer and have long write delay times.

This is a potential problem during a power outage when critical data must be stored into a non-volatile memory immediately. Utility meters may need to record data prior to a power outage. The effects of this data loss can result in significant monetary loss for a utility provider. Fast write speed is a significant feature of F-RAM memory for meter designs.

Since F-RAM memory features high endurance, the system's data can be read and written to F-RAM as though it is general purpose RAM storage inside the host microcontroller. Traditional on-chip RAM provides only temporary storage. And EEPROM offers a limited number of write cycles. F-RAM memory is not only non-volatile but also offers virtually unlimited endurance, eliminating the need for complex wear-levelling software.

F-RAM and Processor Companions for Metering

The use of F-RAM in metering has been widely accepted. Ramtron has developed a set of products that integrate F-RAM and processor companion features. All Ramtron processor companion products integrate F-RAM memory with companion features, such as system reset, power supply voltage detect, watchdog timer, tamper detection, early power fail, and more.

For metering applications, these integrated F-RAM products (**Table 1 below**) not only provide a fast nonvolatile memory but also keep system parts count down, costs down, and reduce board space by including useful features that complement the system microcontroller.

| Features | Benefits |
|--------------------|---|
| Tamper Inputs | Detect/Log Tamper Events |
| Early Power Fail | Write Critical Data Before Main Power is Down |
| System Reset | Low-voltage power supply |
| RTC | Timestamp events |
| Non-volatile F-RAM | Store settings, timestamp, event history, load profiles, etc. |

Table 1. FM31x, FM32x, and FM33x Processor Companions for Metering

Tamper Detect and Event Logging

Event logging and tamper detection are two important features of a meter design. The FM31x devices integrate two 16-bit event counters for tamper-detect or other event logging purposes.

Each counter has an input pin that is edge-triggered and polarity that is user-defined. The event counter may be programmed to detect a tamper event, such as the system's case or access door being opened. The counter is battery-backed so that even when power is lost, the device will detect and count tamper events.

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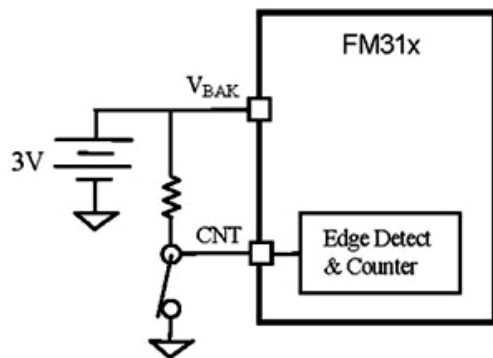


Figure 1. Tamper Detect & 16-bit Counter

In **Figure 1** above, a normally closed switch is shown. The switch is tied to ground, which typically is a system case or chassis. The pullup resistor provides the rising edge when the case or access door is opened.

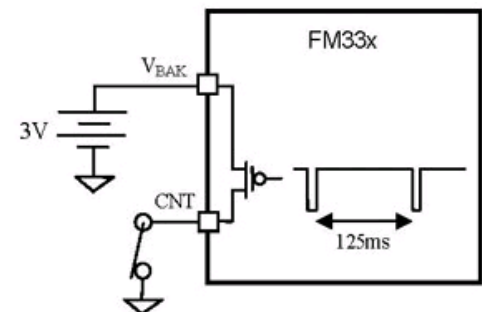


Figure 2. Polled Tamper Detect to Reduce Current

An improved tamper detect circuit is shown in **Figure 2** above. The FM33x devices allow the user to invoke a polled mode, which occasionally samples the pin in order to minimize battery drain. It internally tries to pull the CNT pin up and if an open circuit is pulled up to a VIH level, it will trip the edge detector and increment the event counter value. The current contribution to the meter design is approximately 5nA.

The meter design can also take advantage of the ability of the FM33x devices to store these counts in non-volatile F-RAM. If the design either does not have a backup power source or if the backup source fails, then you still have the counts recorded. No processor overhead is needed.

Early Power Fail Warning

Most electronic systems use voltage-regulated power to provide a stable voltage to guarantee circuit operation. An unregulated power supply always precedes the regulator. As the unregulated voltage varies, the regulated voltage remains stable " to a point.

As the unregulated supply voltage drops, due to a failure or normal system shutdown, the processor and memory subsystem is better served by knowing well before the regulator drop out that power is lost.

An early warning mechanism (**Figure 3** below) provides to the host processor of this event. A non-maskable interrupt (NMI) is a means by which the host can prepare for an impending loss of power.

A simple voltage divider, tied to the unregulated supply, can be connected to the companion's on-chip comparator that senses this condition. The comparator output PFO is tied to the processor's NMI input. This high level interrupt can then invoke a routine that performs a critical task before power is lost.



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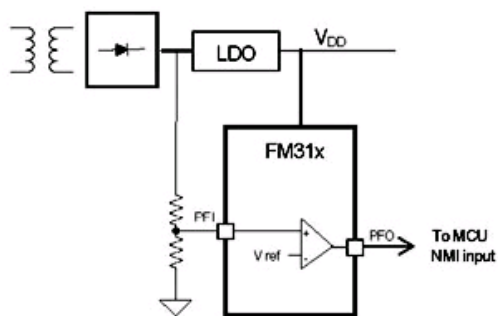


Figure 3. Early Power Fail Warning

System Reset and Voltage Detect

System supervisors typically provide a host processor with the detection of power supply fault conditions and the independent checking of software lockup conditions by using a watchdog timer.

The FM31x, FM32x, and FM33x Processor Companions provide a reset pin (/RST) to drive a processor reset input during power faults, power-up, and software lockups. Whenever the VDD supply is below a user-settable threshold, the low voltage detect circuit holds the system in reset. The reset pin may be wire OR'd with another active-low reset if the design requires it.

Real-Time Clock

A low power, battery-backed real-time clock (RTC) is integrated and can be used in time-of-use (TOU) meters to log power usage overtime. The RTC can be used to timestamp a tamper event or other event. The FM313x and FM33x devices also integrate an alarm which could be useful for setting a flag or future event to trip the host processor.

All RTCs automatically switch over to the backup source when the main power is down. The backed up circuits draw no more than 1microAmpere under this condition. For those designs that cannot use a battery, all Processor Companion devices are able to operate in backup mode from a super capacitor. An integrated capacitor charging circuit is provided on all companion devices.

Mike Peters is a Sr. Applications Engineering Manager at Ramtron International of Colorado Springs, CO. He held the position of chairman of the JEDEC JC42.2 SRAM committee. He holds five US patents and a BSEE from the University of Michigan, Ann Arbor, MI.

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