

VRS51L3074 and serial F-RAM in LED display monitor application

[machine translation for original Chinese article]

Monolithic integrated circuit and embedded system application

Southwest Jiaotong University, Jin Weili black horse Wu Zhiquan

VRS51L3074 is section running rate attainable 40MIPS's monocycle 8051 microprocessors which Ramtron Corporation produces. VRS51L3074's memory subsystem has 64 KB Flash, 4 352 byte internal SRAM, as well as multitudinous outside suppose the interface. VRS51L3074's high speed enlargement mode SPI interface speed for system clock 1/2, moreover has the multi-byte transmission manually, selects patches or strips of land as worth saving for seed with the output downloading pulse function. These functions regarding directly read in serial Flash using the SPI interface the display data, simultaneously approaches the LED display monitor to transmit very important. The FRAM technology is Ramtron Corporation fuses RAM and the ROM identity, develops has the RAM read-write speed, can fall the storage component which the electricity holds. The FRAM series storage chip has writes the data not to have the time delay, antijamming ability, the FRAM read-write number of times has not limited under 3.3V conditions, data retention time attainable 10~45 year and so on multitudinous merits. The FRAM product has provided many kinds of interfaces (for example I2C, SPI, parallel interface), many kinds of capacities (4Kb, 16 Kb, 64 Kb, 256 Kb, 1 Mb and so on), many kinds of voltage rank product. FM25L256B is 32K×8 position, has SPI interface FRAM. Because the SPI bus is a four-wire system, has when SPI interface FRAM frame double-end port RAM, the data line and the pilot wire switch is extremely convenient, therefore uses FRAM to become frame the large capacity double port RAM best selection.

1 LED display monitor control system to serial FRAM requirement

First, 3 FRAM composition data processing system and the FRAM link relations which checks to VRS51L3074 carries on the analysis. Chart 1(a) for VRS51L3074 and 3 FRAM composition data processing system. When carries on the display data processing the SPI bus for the standard link form, namely all SPI interface chip SI, SO, SCK links separately in together; Only then selects patches or strips of land as worth saving for seed the line segment not to link with VRS51L3074, carries on the read-write operation separately to each memory data. When data display only needs the synchronization to assign 3 serial storage same start address, then foot sends in 74HC164 in under the SCK pulse function by serial FRAM the memory SO, and converts the direct output LED display monitor after the string. As a result of display data directly by 74HC164 bypass "DMA" to LED display monitor, therefore does not need to process the serial storage as data display check VRS51L3074 the output data, in other words only needs to 3 serial storages to carry on the open-loop control. Specific electric circuit diagram like chart 1(b) shows.

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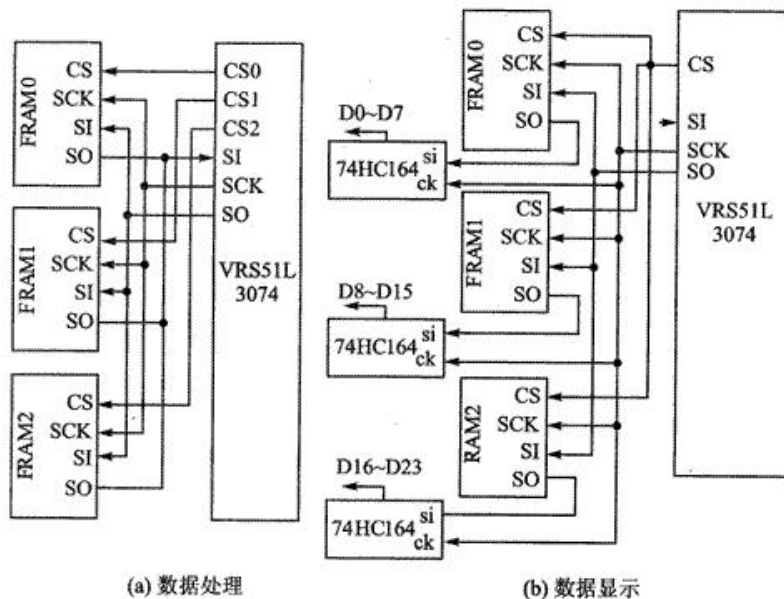


图 1 存储器连接形式与数据管理和数据展示的关系

2 pair of port RAM module and LED display monitor control system

Shown in Figure 2 the serial double port RAM module is acts according to Figure 1 data processing and the data display SPI link relations, sur- bus switch 74HC245 frame. SPI interface FRAM clock signal SCK and data input end SI uses in common, but because actuates time the LED display monitor 3 select patches or strips of land as worth saving for seed the signal to have also to be valid, the data output SO end (e.g. chart 1(b) shows, meets 3 piece of 74HC164's input ends also to need the independent control separately), therefore needs by 74HC245 bus switch implementation the check signal which in port A, B switches to be 8 (SI,1; SCK,1; CS,3; SO,3), used 2 piece of 8 bus data switch 74HC245 to be enough.

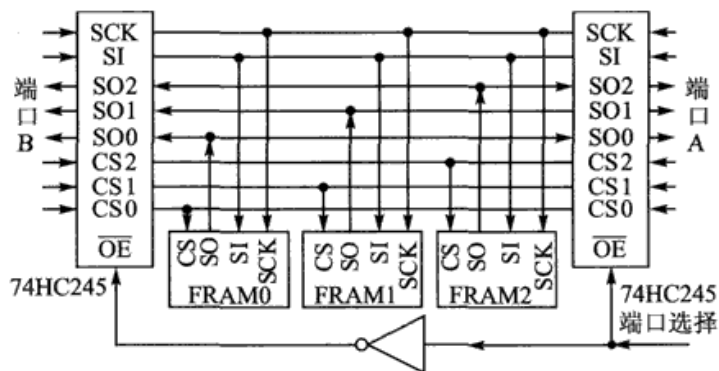


图 2 由串行 FRAM 组成的双端口 RAM 模块

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Figure 3 is the LED display monitor control system which frame by 2 serial double port RAM module. When work the data processing monolithic integrated circuit and the data display monolithic integrated circuit carries on the synchronized work through 2 pilot wires, in which data processing monolithic integrated circuit is the host computer, the data display monolithic integrated circuit for from computer. In the practical application, may through adding serial double port RAM module quantity, or adds 74HC164's progression to add the LED display monitor the altitude. LED display monitor horizontal direction length only with data display monolithic integrated circuit as well as serial FRAM SPI clock frequency related, when the SPI clock frequency is 20 MHz, horizontal direction length attainable 2 048. Under bidirectional actuation model, LED display monitor highly by serial double port RAM module quantity determination. Horizontal direction length when 40 MHz does not have the gradation attainable 4 096, in 8 level of gradation situations attainable 512 points; But vertical direction 3 piece of FRAM and converts after 74HC164 string 3 bytes (altogether 24 bits), double color points = $24 \div 2 \times 16 = 192$ point, monochromatic points = $24 \times 16 = 384$ point.

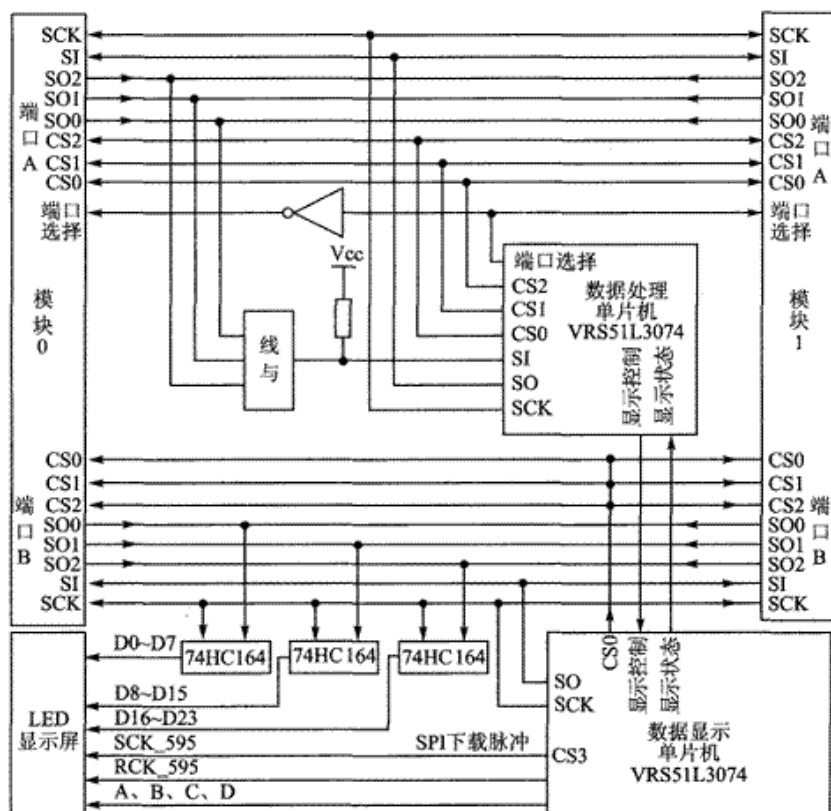


图 3 基于串行双端口 RAM 模块的 LED 显示屏控制系统

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FM25L256B serial FRAM read-write with serial Flash basic consistent. After the most major characteristic is writes a byte not to need to look like the serial Flash such inquiry to write operates whether completes, but is the elephant sequentially reads the operation to write equally continuously; Also does not need to erase first reads in again, also does not have the read-write number of times limit, definitely may look like the RAM same use. VRS51L3074's SPI interface speed for system clock 1/2, the common 51 monolithic integrated circuit SPI interface speed all is the system clock 1/4 (has not downloaded pulse), therefore VRS51L3074's SPI interface certain identities have the extremely vital role in the LED display monitor control system. Similarly, serial FRAM and VRS51L3074 frame together the double port RAM control system, may complete the multi-bytes extremely conveniently using VRS51L3074's SPI interface read-write.

3 pair of MCU uses in common the double port RAM joint operation

First, the data processing monolithic integrated circuit in 1 organizes the similar display data in module O and the module, then through display control end start data display monolithic integrated circuit. The data display monolithic integrated circuit to the authority which serial FRAM only then reads, only can simultaneously select patches or strips of land as worth saving for seed module 0 or 1 3 piece of FRAM through CS0, and simultaneously gives in module O or 1 3 piece of FRAM through the SO end delivers the display data the first address; Then under the SCK function, module O or 1 3 piece of FRAM to corresponds 74HCl64's SI end output display data through respective SO end, simultaneously automatedly produces the shifting pulse by the data display monolithic integrated circuit through CS3 end which the LED display monitor single disc needs. Completes after LED display monitor line of displays, the data display monolithic integrated circuit sends to the data processing monolithic integrated circuit goes on a journey the state signal which the display completes, simultaneously waited for the data display monolithic integrated circuit sends out the instruction which continues to display, after receives continues the display command the start next line of displays. The data processing monolithic integrated circuit may according to need to let data display monolithic integrated circuit display module O or 1 display data through the port selection, also the monolithic integrated circuit may which displayed while the data display monolithic integrated circuit, processes the double port RAM module 1 or in the O display data.

Conclusion

This article was composed double-end port RAM to the LED display monitor control system use by the serial FRAM memory the hardware system and the control method has carried on the preliminary discussion. This kind of double port RAM and the traditional double port RAM similarity lies in its port an end to be possible read-write, but another end only can read. Uses serial FRAM to compose double-end

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port RAM to have the pilot wire few, the capacity big and the price low status merit, is not in the very high situation has the good application foreground in the read-write speed requirement.

References

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Source: *Chinese LED network* (<http://www.cnledw.com/technique/detail-17343.htm>)