

F-RAM Ideal for Next Generation Cellular Phones

Cellular phone designers are under constant pressure to develop low cost, low-power, high content electronics in an ever-shrinking package. With nearly all major phone manufacturers working towards similar goals with similar tools and building blocks, it comes as no surprise that most phones today both look and work alike. And, given similar pricing strategies, it's no wonder that product differentiation is often the final arbiter in the consumers' decision making process. Being different in the right way at the right time is the key to capturing the market share in any segment.

F-RAM memory offers the cellular phone designer several advantages over the traditional nonvolatile memory which can be leveraged to create features that noticeably differentiate their product from the competition.

Why Use F-RAM?

F-RAM, available from Ramtron International Corporation, is a non-volatile RAM. Read and write operations are symmetric and endurance is virtually unlimited. In the past, system designers were forced to use electrically alterable PROMs (FLASH / EEPROM) in applications where non-volatile RAM is better suited.

- F-RAM's low-power symmetrical read/write operation is easy on batteries. The energy used to write a single byte of EEPROM is enough to write fifty thousand bytes of F-RAM.

- F-RAM is many times faster than FLASH or EEPROM, with an average speed of 46ns per read/write cycle and no wait times.

- F-RAM's endurance is virtually unlimited at 10^{15} read/write cycles, or one billion times the life of the EEPROM.

- F-RAM is reliable. Your data is stored as a state, not as a charge like EEPROM and FLASH devices. It is not susceptible to single event upsets or

magnetic fields. F-RAM even offers resistance to memory corrupting Gamma radiation.

Applications

- Extend 'stand-by' time** by substituting F-RAM for SRAM or SDRAM. F-RAM consumes as little as 5µA in sleep mode and the application micro-controller can be powered off during periods of inactivity.

- Eliminate delays during power-up** by substituting F-RAM for SRAM or SDRAM. F-RAM enables the highly desirable "instant on" feature in your cell phone design by powering up with the last known data fully intact. See Figure 1 Generic Cellular Phone Functional Block Diagram.

- Eliminate GPS signal acquisition delays** by storing the GPS data stream and localized map data in F-RAM. At start-up, the GPS application reads back the last position and displays the map data, allowing instant access to the user's desired location data.

- Eliminate the need for wear-leveling** techniques used in solid-state storage by storing file entry points and other frequently updated data in F-RAM while the bulk data remains in low endurance FLASH.

- Enhance multimedia playback** by caching decompressed stream data in F-RAM, allowing for instant resumption of playback during power-up or wake events.

- Enhance security** by storing sensitive information in an AES secured F-RAM. Secured F-RAM requires the host processor to verify its identity using the AES encryption protocol before data exchange can take place. Multiple failed attempts or an external tamper signal will cause the memory to be erased entirely. Once authenticated, the data is made available to the MCU in plain text, to reduce processor overhead.

Contact your Future Electronics sales representative today to find out how Ramtron's F-RAM nonvolatile memory can take your next cell phone design to a new level of excellence.

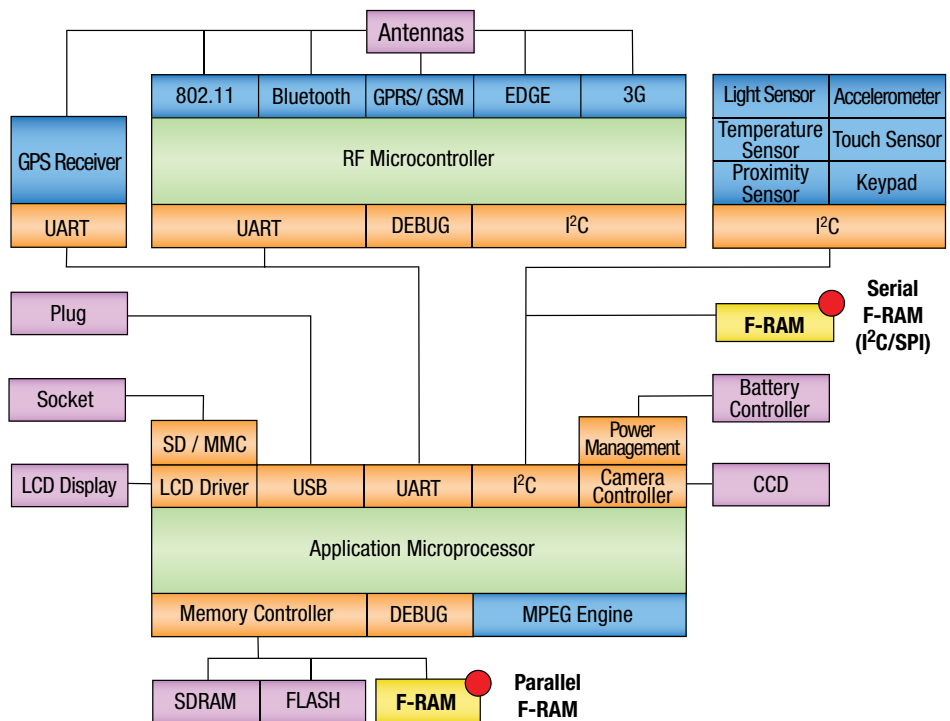


Figure 1. Generic cellular phone functional block diagram



[Click here to buy this product](#)

Ramtron F-RAM

Using Op-Amps in the Precision Signal Path: A Guide for the Digital Engineer

By Jose Perez, FAE, Future Electronics (Spain)

READ THIS TO FIND OUT ABOUT

- Analog signal conditioning
- Precision op-amp selection
- Designing op-amp circuits

In the past 20 years, developments in electronics have primarily been seen in the digital domain. Modern mixed-signal ICs have even replaced many traditional analog implementations. But despite this, pure analog hardware continues to have its place in many systems. This article explains how digital engineers can tackle analog design.

A common example is the signal path in a typical control or instrumentation system. Here, the sensor signal generally requires some kind of conditioning before it can drive an ADC. Nowadays, the task of designing this analog circuit, usually based on an op-amp, is only a small part of the whole system design. This means that engineers working primarily in the digital domain will often be required to perform this task.

Precision Signal Path

A precision signal path can be defined as a signal path with an input offset voltage (V_{OS}) of less than 1mV. When designing such a precision signal path, the overall strategy is to reach the required precision by controlling each individual source of error. These sources are the main components of what is known as the error budget equation, which can be used when designing a signal-conditioning block.

Signal-Conditioning Block

Typical functions performed by the signal-conditioning block include amplification, level shifting, buffering and filtering. With the sensor already characterized and the ADC selected, it will be clear which of these are required in order to match the sensor output to the ADC (see Figure 1).

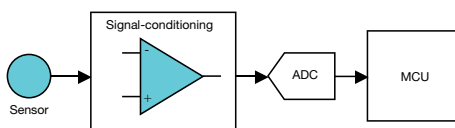


Figure 1. Typical signal-conditioning application

At this point, the error limit is usually set in terms of the Least Significant Bit (LSB) of the ADC. Then, by considering the function's requirements and the maximum error allowed, the process of op-amp selection can start.

Single Supply Op-Amp Selection

Selecting a single supply op-amp that operates at the same power supply voltage (V_{DD}) as the ADC, can reduce part count and cost. When using a single supply device, the first consideration is its behavior under input common-mode voltages (V_{CM}). Single supply op-amps can manage input voltages close to one of the power supply rails, either ground or V_{DD} , but typically no closer than 1V from the opposite rail. Alternatively, other single supply devices such as Rail-to-Rail Input (RRI) op-amps are able to accept input voltages close to both supply rails.

However, the input-stage structure of RRI op-amps means that their input offset voltage shows a relatively large variation, sometimes even in polarity, as V_{CM} swings from one rail to the other. In these kinds of op-amps, the effect of common-mode voltages on input offset voltage must be considered. In most applications, the RRI feature is not absolutely essential; if this is the case, it is better to choose a single supply op-amp that keeps V_{CM} close to the appropriate rail.

In addition to considering the input voltage values, the output characteristics must be evaluated. To take advantage of the ADC's complete dynamic range, the op-amp output must match the ADC's reference voltage (V_{ref}) value. This frequently makes the use of rail-to-rail output op-amps mandatory.

Op-Amp Error Budget

The major op-amp parameters that affect precision are:

- Input offset voltage (V_{OS}) and drift (dV_{OS}/dT)
- Common-Mode Rejection Ratio (CMRR)
- Power Supply Rejection Ratio (PSRR)
- Open-loop voltage gain (A_{VOL})
- Input bias current (I_B)
- Bandwidth
- Noise

To analyze the parameters above, the following equation is used, with the output error given by V_{IN} multiplied by the gain. It is important to note that external components around the op-amp would also affect circuit behavior.

$$v_{in,d} = \frac{v_o}{A_{vol}} + V_{os} + (I_{B+}) R_{s+} + (I_{B-}) R_{s-} + \frac{v_{CM}}{CMRR}$$

It is clear from the above equation that the output error can be managed by separately managing each of the individual components of the error budget. This article will now examine each in turn.

Gain Error

Consider the well-known closed-loop gain expression:

$$A_{CL}(\omega) = A_0(\omega)/(1+A_0(\omega)\times\beta)$$

Where $A_0(\omega)$ = open-loop gain

β = feedback factor (resistive in this case)

It can be noted that if $A_0(\omega)$ varies, then A_{CL} will vary, as will the output voltage. The $A_0(\omega)$ variation can come from frequency dependency or DC-gain variations.

Although, in precision applications, the signal frequency could be low, the amplifier bandwidth must be considered, since the closed-loop bandwidth must be wide enough to avoid attenuating any frequency components. As most of the op-amps use dominant-pole compensation, the bode plot is the same as for a single-pole filter (-20dB/dec).

The frequency at $A_0(\omega) = 1$ is specified in the datasheet; this is known as the Gain-Bandwidth Product (GBWP) and can be used to obtain the closed-loop bandwidth:

$$BW_{CL(-3dB)} = GBWP/A_{CL}$$

For example, an op-amp with a 6MHz GBWP, configured with a gain of 10, will have a closed-loop bandwidth of:

$$BW_{CL(-3dB)} = 600kHz$$